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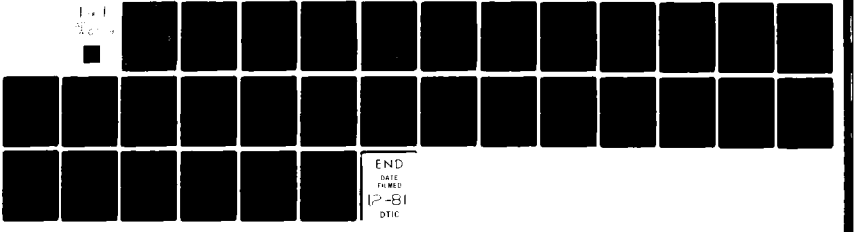

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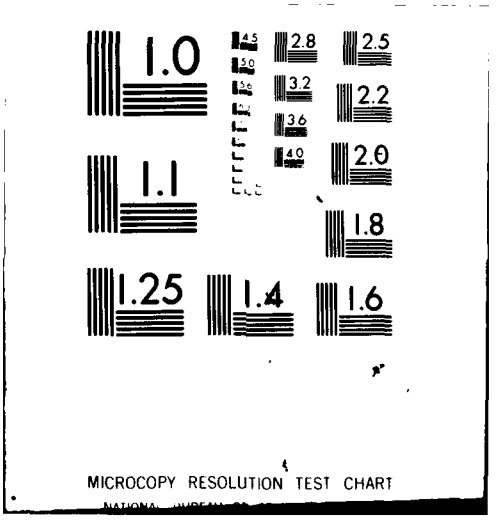
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# TECHNICAL REPORT

## STEWS – ID – 81 – 2

# IRIG – TIME SYNCHRONIZED BINARY VIDEO DATA INSERTER



SEP 1981

FINAL REPORT





INSTRUMENTATION DIRECTORATE
US ARMY WHITE SANDS MISSILE RANGE
WHITE SANDS MISSILE RANGE, NEW MEXICO 88002

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| REPORT DOCUMENTATION PAGE | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|
| 1. REPORT NUMBER: STEWS-ID-81-2 | 2. GOVT ACCESSION NO.: AD-A107 119 |
| | 3. RECIPIENT'S CATALOG NUMBER |
| 4. TITLE (and Subtitle): IRIG-TIME Synchronized Binary Video Data Inserter | 5. TYPE OF REPORT & PERIOD COVERED: Final Report |
| | 6. PERFORMING ORG. REPORT NUMBER |
| 7. AUTHOR(s): Federico Salvatti, Jr. - STEWS-ID-O, WSMR, NM | 8. CONTRACT OR GRANT NUMBER(s) |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS: Commander, US Army White Sands Missile Range, ATTN: STEWS-ID-O, White Sands Missile Range, New Mexico 88002 | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: DA Project No. 10024E |
| 11. CONTROLLING OFFICE NAME AND ADDRESS | 12. REPORT DATE: SEP 1981 |
| | 13. NUMBER OF PAGES: 22 |
| 14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) | 15. SECURITY CLASS. (of this report): UNCLASSIFIED |
| | 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Video synchronizer
Binary video inserter
IRIG-B Synchronized
Phase-locked loop

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Binary Video Inserter (BVI) was developed to insert binary data into a video signal. A Video Synchronizer was developed to synchronize the BVI to IRIG-B range time. The combination provides a Synchronized Binary Video Inserter (SBVI) in support of a program to replace film-based mobile cine-theodolite instrumentation presently in use at WSMR. The SBVI satisfies the

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following objectives:

(1) Synchronizes shuttered video cameras to IRIG-B time.

(2) Provides timing and control signals to achieve high frame rate capability for recording launch area and miss distance event data.

(3) Insert time, instrument encoder data, and other data into the video signal for computer-assisted processing.

(4) Provide error recovery capability for the inserted data.

## ACKNOWLEDGEMENTS

The development of the IRIG-Time Synchronized Binary Video Data Inserter was an iterative process. Mr. Charles Tapp and Mr. John Morgan provided the initial feedback that is necessary to develop a field-worthy product. Immunity to time base error and data error recovery are features that were added as a result of their suggestions.

The discussion on synchronizing color and monochrome TV cameras resulted from conversations with Messrs. Charles Tapp, Clifford Horn, and Bob Lockyear.

Finally, this report was made possible by the dedicated typing efforts of Mrs. Helene Essary and the drafting skills of Mr. Manuel Ramos.

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## INTRODUCTION

The Synchronized Binary Video-Data Inserter (SBVI) was designed to be compatible with the Video Image Analysis System presently in use at WSMR and is an option that fits in the Digital Tracking Filter (DTF) which controls the servo drive on WSMR optical tracking systems. The SBVI is part of a long-range program to lower operating costs of optical instrumentation systems by replacing film with video tape and providing quick response to the customer's data needs by automating the data processing wherever possible. The SBVI consists of a Video Synchronizer and a Binary Video-Data Inserter together which satisfy the following objectives:

(1) Synchronize shuttered video cameras to IRIG-B time.

(2) Provide high frame rate video capability for recording launch area and miss distance event data.

(3) Insert time, instrument encoder data, and other data into the video signal for computer-assisted processing.

(4) Provide error recovery capability for the inserted data.

## GENERAL DESIGN CONSIDERATIONS

The modulation method selected for inserting data on the video signal is based on the requirements that the data be:

- Compatible with existing video analysis equipment.
- Immune to time-base error.
- Immune to burst-noise errors.
- Compatible with color or monochrome CCTV.
- Hardware compact.

To avoid building hardware decoders initially, it was decided to decode the inserted data using software on the existing video analysis equipment. From a software point of view pulse amplitude modulation (PAM) is easier to handle than either pulse width, PCM, or frequency modulation. A large amplitude pulse is used to represent a binary "one" and a small amplitude pulse to represent a binary zero. Although only RS-170 standard video cameras are used, signal amplitudes vary from camera to camera. Binary pulse amplitudes have to maintain a constant relationship to the incoming video signal amplitude. This relationship is preserved by making the pulse heights multiples of the difference between video blanking level and sync level.

Immunity to time-base error is acheived by placing a data pulse at the trailing edge of each horizontal blanking interval. Data is extracted by detecting the first non-black video level at the trailing end of the horizontal blanking interval. This level is compared to a threshold level lying halfway between maximum binary data and non-binary video peaks. This method of detection also provides protection against varying video signal amplitudes due to magnetic tape or recorder imperfections.

The position of the data pulses, together with the modulation scheme, insures compatibility with color or monochrome video and avoids the destruction of information when the signal is regenerated by time-base correction equipment.

Error recovery is provided by insuring that only single-bit errors will be likely to occur. This objective is attained by placing only one bit of information on each horizontal line, thus avoiding burst-noise induced multiple errors. Single-bit error recovery is provided by Hamming coded data. Four Hamming bits are used for each eight bits of data.

## DATA CAPACITY

The binary data is written onto the video signal in bit-serial format. The first two words are used for field synchronization. Each word is twelve bits long, consisting of eight bits of data and four bits of Hamming code. The third word is a field identifier with a total of 256 uniquely identified video fields possible before the field ID repeats.

A maximum of 21 words can be written in each field; therefore each field will contain 2 sync words, 1 field identifier word, and 18 data words. There are 21 x 12 = 252 usable video lines per field. This information is summarized below:

FORMAT

| WORDS | 2 | 1 | 18 |
|---|---|---|---|
| FUNCTION | Sync | Field | Data |

DATA CAPACITY

| | |
|---|---|
| Usable lines per field | 252 lines |
| Data Bits per word | 8 Bits |
| Hamming Bits per word | 4 Bits |
| Word - Data + Hamming | 12 Bits |
| Words per Field | 21 Words |

## ON BOARD MICROCOMPUTER

The BVI is an intelligent peripheral to the DTF. An embedded single chip micro-computer gathers time information, servo encoder data, and housekeeping data and reformats it for use by the data reduction computer. The micro-computer also makes the BVI adaptable to changing requirements in the field -- without changing the hardware. In addition, the use of the single-chip microcomputer was a key factor in packaging the BVI in a single module.

## VIDEO SYNCHRONIZATION

Video instrumentation cameras are operated in the external sync mode. A composite sync signal is generated externally and phase-locked to the basic 6 MHz clock in the timing unit. Thus, the video signal is phase-locked to every output of the timing unit. The composite sync is coincident with 10 Hz, thus video data is synchronous with servo encoder data sampled at any multiple of 10 Hz.

A byproduct of synchronization is the ability to produce high frame-rate video data using phased camera arrays. The video synchronizer is designed to provide up to a maximum sampling rate of 240 fields-per-second.

## FUNCTIONAL DESCRIPTION

### OVERVIEW

Figures 1 and 2 illustrate how the SBVI fits into the control scheme of the optical tracking instrument, and the input and output signals required.

Figures 3 and 8 are simplified block diagrams of the video synchronizer and the BVI, respectively. The discussion to follow will be based on these block diagrams and associated timing diagrams.

### VIDEO SYNCHRONIZER

The video synchronizer (VS) takes three signals from a standard timing unit which is locked to IRIG-B. All timing unit output signals are derived from its basic 6 MHz internal oscillator. The VS synthesizes a 1.26 MHz clock which is required by commerically available TV camera sync generators. This clock is phase-locked to the 6 MHz timing unit oscillator; hence it is locked to 2400 Hz and 10 Hz timing unit outputs.

The 2400 Hz signal is used to provide a basic 240 PPS count pulse to a four-state counter which, together with a 2- to 4-line decoder, provides four phases of vertical-reset signals. Each vertical-reset ($\overline{VR0}$ thru $\overline{VR3}$) signal occurs 30 times per second, and is used to synchronize four different TV camera sync generators operating in the interlaced mode (see Figure 4). The $\overline{VR0}$ through $\overline{VR3}$ vertical reset pulses must satisfy the timing relationship with the 1.26 MHz clock shown in Figure 4a. Figure 4b shows how each of the four VR signals can be used to achieve an effective 240 fields-per-second (fps) video rate using four different cameras, each synchronized to its own TV camera sync generator. Figure 5 shows how this array of cameras could be used to produce high frame-rate video, using conventional video equipment. The video data from each camera can be recorded separately, and later merged into a single video tape. This single tape can then play back the merged video, producing a slow-motion effect of the 240 fps viewed at 60 fps.

The computer-controlled video editor will be designed locally because it must use the inserted time data to sequence the four-tape recorders in the proper order -- one field at a time.

#### Phase-locked loop

The action of the phase-locked loop (PLL) is to synthesize 1.26 MHz from 6 MHz. It does so by forcing the output frequency divided by 21 to equal the input frequency divided by 100:

$$\frac{6\ \text{MHz}}{100} = \frac{1.26\ \text{MHz}}{21} = 60\ \text{KHz}$$

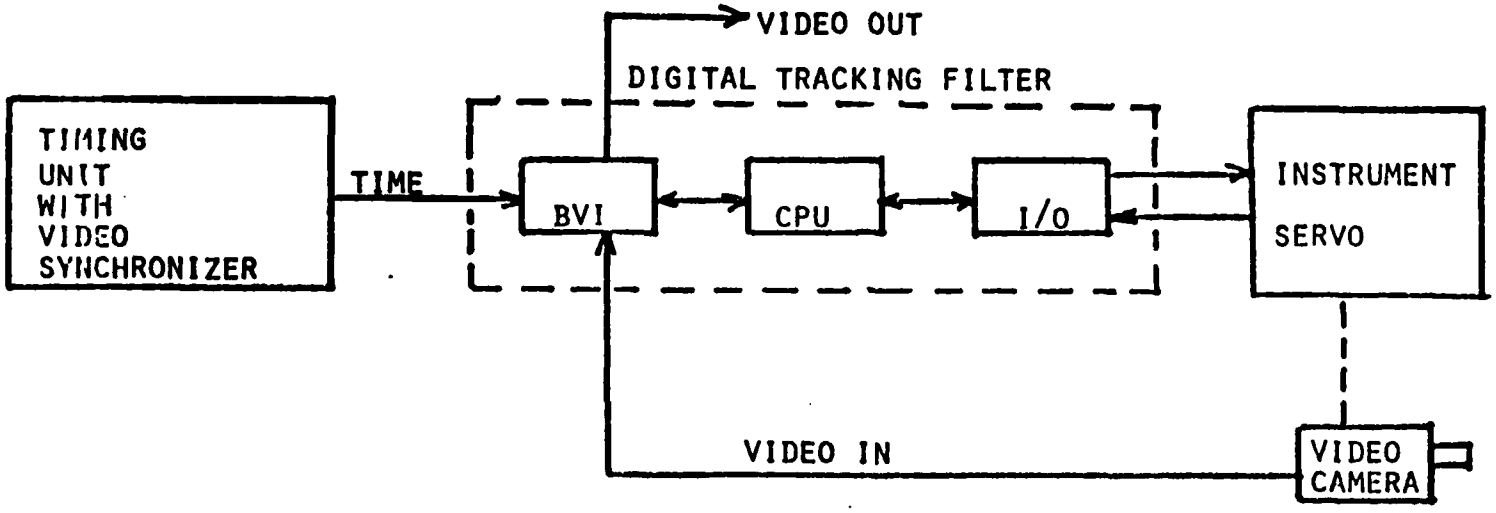



Figure 1. BVI option to the digital tracking filter.

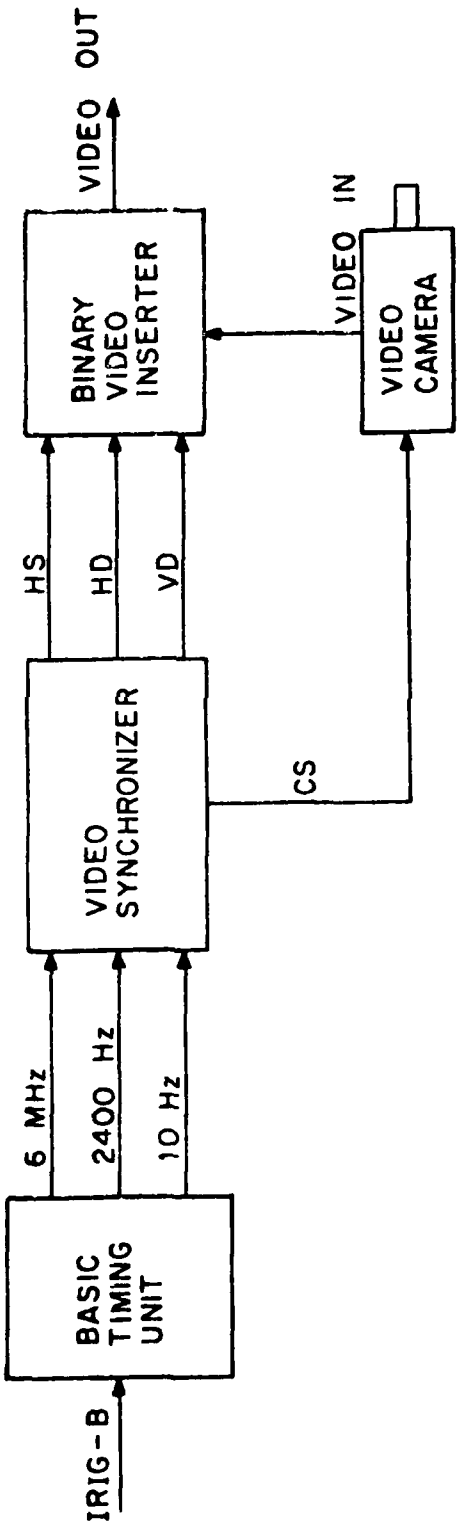



Figure 2. IRIG-B synchronized binary video inserter.

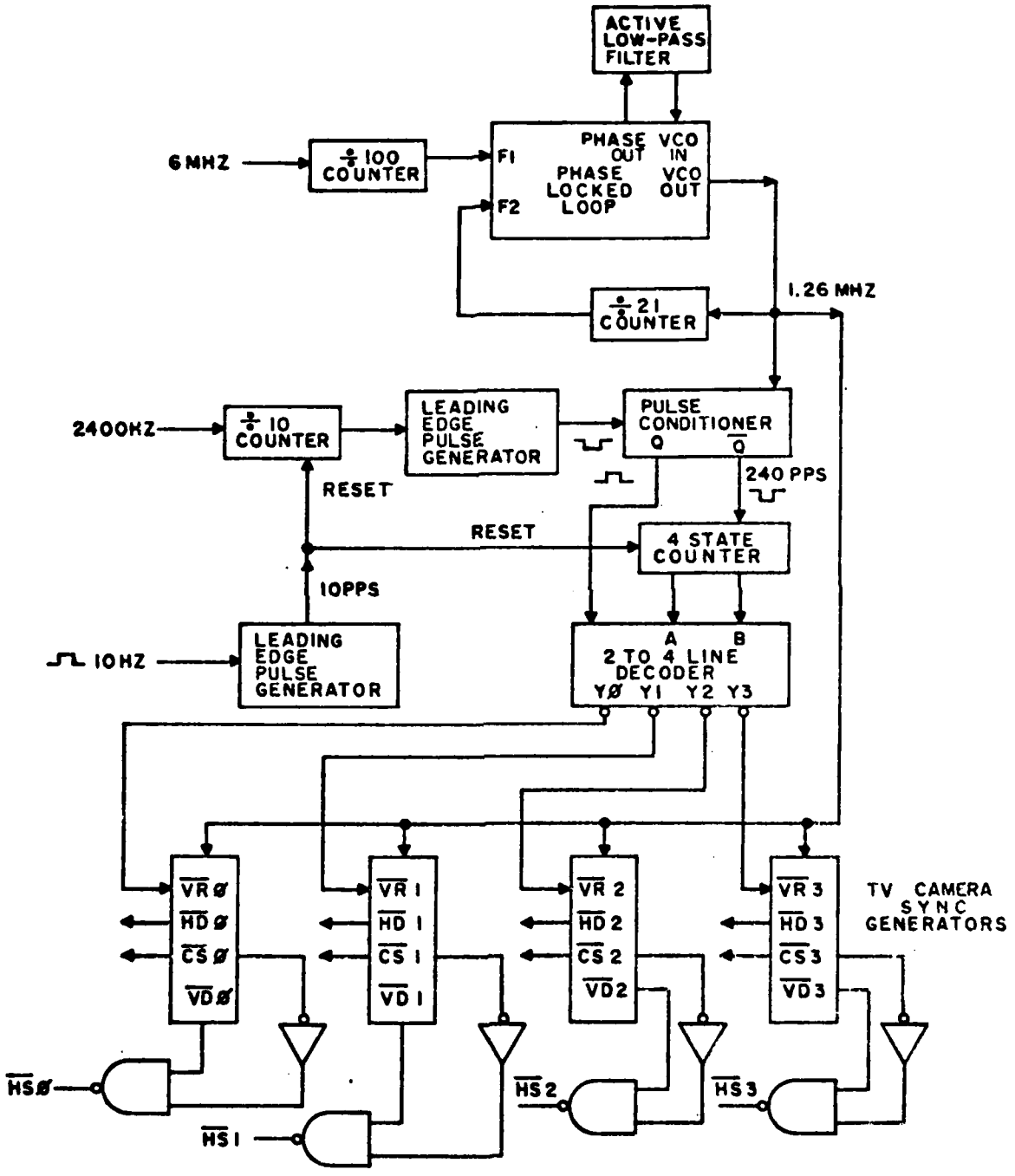
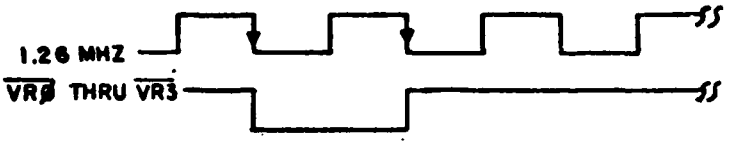
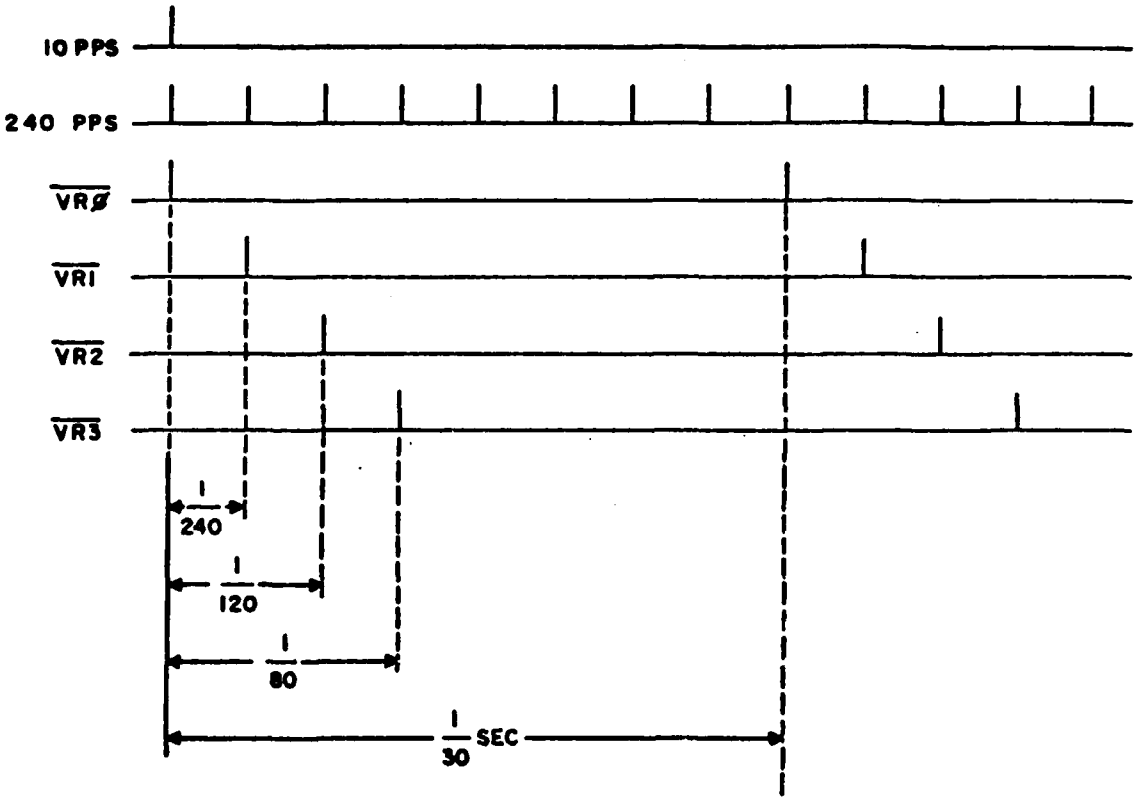



Figure 3. Video synchronizer.




(a)




(b)

Figure 4. Video synchronizer timing diagram.

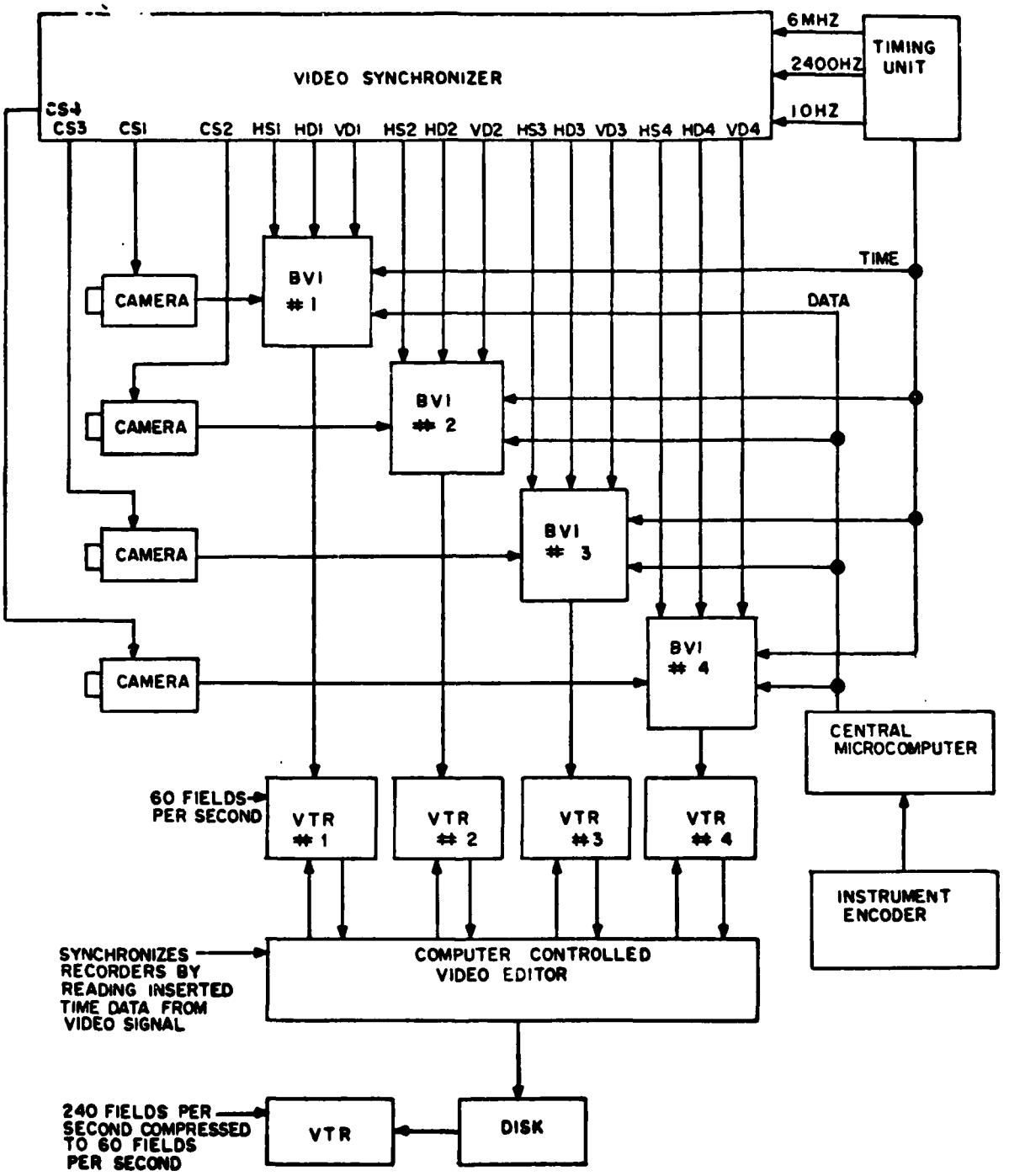



Figure 5. Phased camera array video instrumentation system.

A type 2, second-order PLL[1] was designed, based on a desired settling Time ($T_s$) of 10 milliseconds. The system stability requirement, expressed as a ratio of system time constant to the period of the system damped natural frequency, was chosen to be $\left(\frac{\tau}{\tau_d}\right) = 1$.

Using available components, the actual performance was:

$T_s = .04$ seconds

$\frac{\tau}{\tau_d} = 1.4$

The stability factor can be expressed in terms of the conventional second order damping factor:

$$\left(\frac{\tau}{\tau_d}\right) = \sqrt{\frac{1}{\zeta^2} - 1} \tag{1}$$

where

$$\tau = \frac{1}{\zeta w_n} \tag{2}$$

$$w_d = w_n \sqrt{1 - \zeta^2} \tag{3}$$

$$\tau_d = \frac{1}{w_d} \tag{4}$$

A value of $\frac{\tau}{\tau_d} = 1$ corresponds to $\delta = .707 = \frac{1}{\sqrt{2}}$

Settling time $T_s$ is equal to the number of cycles of $w_d$ per time constant, times the period of the damped natural frequency:

$$T_s = \left(\frac{\tau}{\tau_d}\right) T_d \tag{5}$$

where

$$T_d = \frac{2\pi}{w_d} \tag{6}$$

so that

$$T_s = \left(\frac{\tau}{\tau_d}\right) \frac{2\pi}{w_d} = \left(\frac{\tau}{\tau_d}\right) \frac{2\pi}{w_n \sqrt{1 - \zeta^2}}$$

Substituting $\zeta^2$ in terms of $\left(\frac{\tau}{\tau_d}\right)$

$$T_s = \frac{2\pi}{w_n} \sqrt{\left(\frac{\tau}{\tau_d}\right)^2 + 1}$$

---

[1] Gardner, F. M., Phaselock Techniques, New York, McGraw-Hill Book Company, Inc., 1966.

Solving for $w_n$:

$$w_n = \frac{2\pi}{T_s}\sqrt{\left(\frac{\tau}{\tau_d}\right)^2 + 1} \qquad (7)$$

Equation (7) can be used, together with equations (8) and (9) derived from Figure 6, to obtain the relationship between the filter components and the desired performance characteristics.

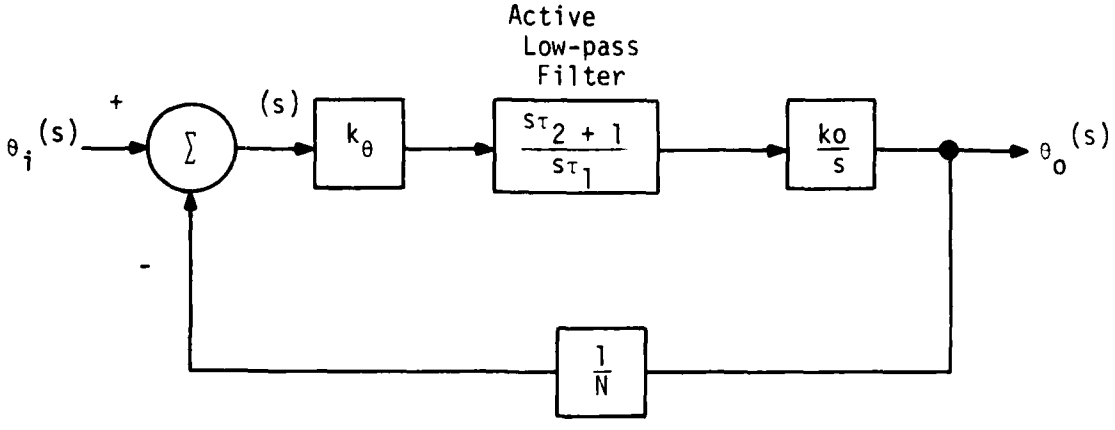



Figure 6. Transfer function diagram of PLL.

$$\frac{\varepsilon(s)}{\theta_i(s)} = \frac{1}{1 + G(s)\,H(s)} = \frac{1}{1 + \frac{k_\theta k_o}{s^2\tau_1 N}(s\tau_2 + 1)}$$

$$= \frac{s^2\tau_1 N}{k_\theta k_o(s\tau_2 + 1)\left(\frac{s^2\tau_1 N}{k_\theta k_o(s\tau_2 + 1)} + 1\right)}$$

$$= \frac{s^2\left(\frac{\tau_1 N}{k_\theta k_o}\right)}{\left(s^2\frac{\tau_1 N}{k_\theta k_o} + s\tau_2 + 1\right)}$$

The denominator is of the form $s^2 \frac{1}{\omega_n^2} + s \frac{2\zeta}{\omega_n} + 1$

$$\text{whence} \quad \tau_1 = \frac{k_\theta k_o}{N\omega_n^2} = R_1 C \tag{8}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} = R_2 C \tag{9}$$

Tracking error analysis

Taking the series expansion of $\varepsilon(s)$:

$$\varepsilon(s) = \frac{\theta_i(s)s^2}{\frac{k_\theta k_o}{\tau_1 N}} - \frac{\theta_i(s)s^3}{\frac{\omega_n k_\theta k_o}{2s\tau_1 N}} + \ldots \tag{10}$$

or

$$\varepsilon(s) = \frac{s\theta_i(s)}{k_v} + \frac{s^2\theta_i(s)}{k_a} - \frac{s^3\theta_i(s)}{k_j} + \ldots \quad \text{where } k_v = \infty$$

In the time domain

$$\varepsilon(t) = \frac{\dot{\theta}_i(t)}{k_v} + \frac{\ddot{\theta}_i(t)}{k_a} - \frac{\dddot{\theta}(t)}{k_j} + \ldots$$

This means that, under steady-state conditions,

$$k_v = \infty \tag{11}$$

$$k_a = \frac{k_\theta k_o}{\tau_1 N} = \omega_n^2 = \left(\frac{2\pi}{T_s}\right)^2 \left(\left(\frac{\tau}{\tau_d}\right)^2 + 1\right) \tag{12}$$

$$k_j = \frac{\omega_n}{2\zeta}\left(\frac{k_\theta k_o}{\tau_1 N}\right) = \frac{\omega_n^3}{2\zeta} = 4\left(\frac{\pi}{T_s}\right)^3 \left(\left(\frac{\tau}{\tau_d}\right)^2 + 1\right)^{3/2} \tag{13}$$

Since $\theta_i(t) = \omega t$, $\dot{\theta}_i(t) = \omega$, $\ddot{\theta}_i(t) = \frac{d\omega}{dt}$

This loop tracks a constant frequency ($\omega$) with zero error ($k_v = \infty$).

This type of loop can be used to track a constant rate of change of frequency with a constant tracking error. If this were the case, $k_a$ and $\frac{\tau}{\tau_d}$ would be the desired performance parameters.

Since $k_a = f\ T_s, \frac{\tau}{\tau_d}$

then picking $k_a$, and $\frac{\tau}{\tau_d}$ determines what $T_s$ will be.

Active low-pass filter

The choice of a CMOS phase-locked loop and active filter was not arbitrary. Both components were dictated by the sensitivity of the video image to changes in the clock frequency (1.26 MHz) of the TV camera sync generator.

The CMOS PLL was picked because of the characteristics of the edge controlled phase detector. The output goes to a high-impedance state (open switch) condition whenever both input frequencies are in phase. This phase detector thus provides high charging currents, low charging currents or no charging currents to the integrator portion of the low-pass filter (see Figure 7). Active filter (a) is equivalent to active filter (b).

The CMOS phase detector output changes to the high impedance state whenever both inputs to the PLL are equal in phase and frequency. The active filter integrator holds the last value indefinitely without discharging the integrating capacitor. Since the output of the filter is applied to a voltage controlled oscillator (VCO), the VCO output frequency remains constant during the hold time of the active filter. With this approach there is no measurable jitter between the vertical sync and the IO per reference.

A passive filter integrating capacitor cannot hold its charge indefinitely, even when the CMOS phase detector is in the high impedance state. Under steady-state conditions, the capacitor of the passive filter will constantly charge and discharge to achieve an average d.c. voltage which corresponds to the desired output frequency from the VCO. The average frequency out of the VCO will be 1.26 MHz, but the instantaneous frequency will be sweeping slightly above and below this average frequency. If this frequency were applied to the TV camera sync generator, the resultant TV image would alternately be expanded and compressed from hornizontal line to horizontal line. For this reason a passive filter was not used.

Synchronizing color and monochrome TV cameras

There could be a problem if both monochrome and color cameras were used in the field, each running at its own standard vertical sync rate (59.94 Hz for color and 60 Hz for monochrome). Both camera systems would not remain synchronized to each other, though each would be synchronized to a timing unit.

The slower frequency would fall behind $\Delta T$ seconds each cycle. If T is the period of the higher frequency, then after $\frac{T}{\Delta T}$ cycles of the slower frequency, the two frequencies would be phase-coincident again.

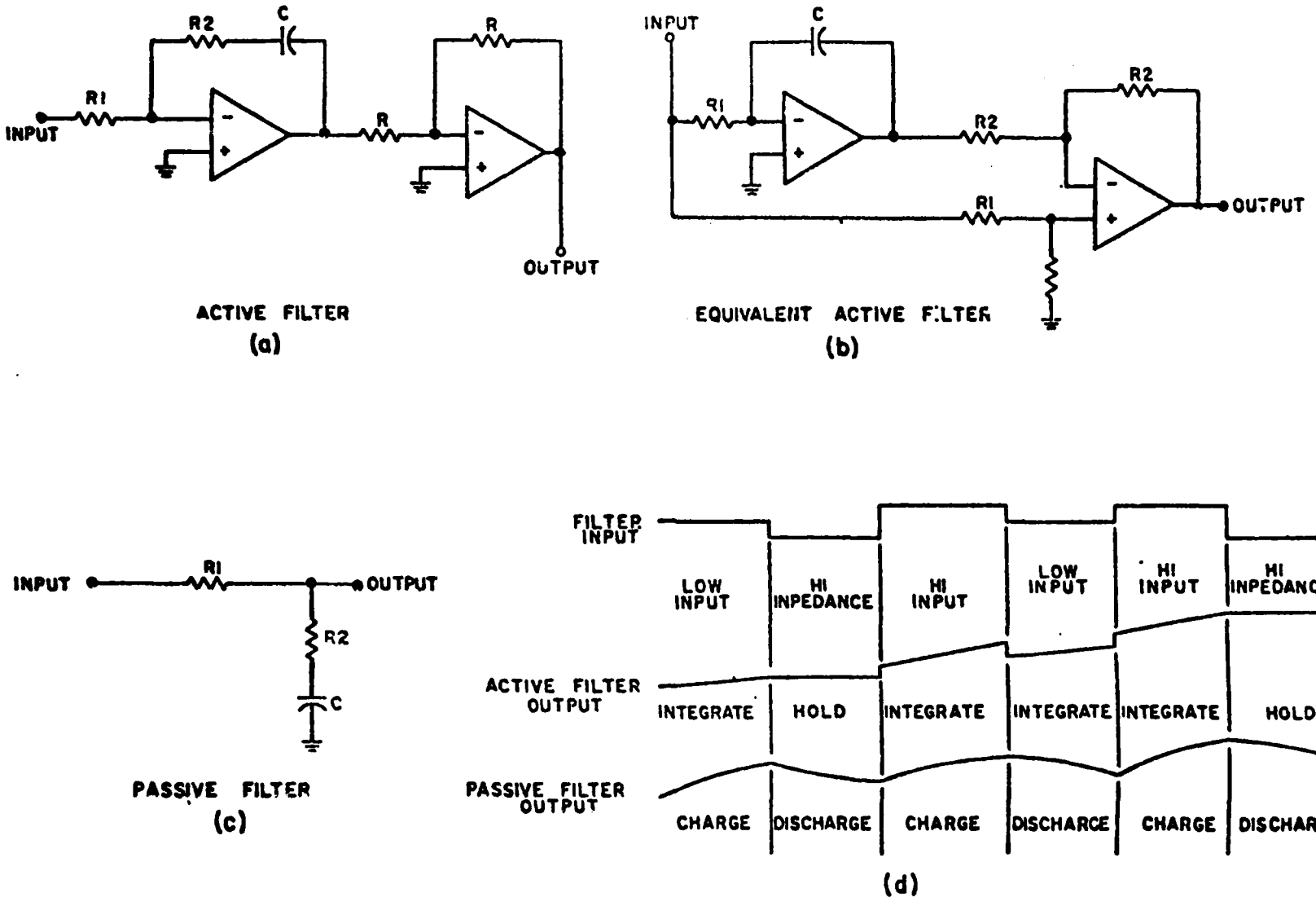



Figure 7. Active low pass filter.

$$\frac{T}{\Delta T} = \frac{\frac{1}{f_2}}{\frac{1}{f_1} - \frac{1}{f_2}} = \frac{1}{\frac{f_2}{f_1} - 1}$$

where $f_2 > f_1$

The time required for $\sin 2\pi f_1 t$ to slip behind one cycle of $\sin 2\pi f_2 t$ would be

$$\left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\left(T_1\right) = \left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\frac{1}{f_1} = t$$

and at this point in time, $\sin 2\pi f_1 t = \sin 2\pi f_2 t$.

Substituting for t: $$\sin\left[2\pi f_1\left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\frac{1}{f_1}\right] = \sin\left[2\pi f_2\left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\frac{1}{f_1}\right]$$

or $$\sin\left[2\pi\frac{1}{\frac{f_2}{f_1} - 1}\right] = \sin\left[2\pi\frac{f_2}{f_1}\left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\right]$$

Looking at the right side of this equation:

$$\sin\ 2\pi\left[\frac{\frac{f_2}{f_1}}{\left(\frac{f_2}{f_1} - 1\right)}\right] = \sin\left[2\pi\frac{\left(\frac{f_2}{f_1} - 1\right) + 1}{\left(\frac{f_2}{f_1} - 1\right)}\right] = \sin\left[2\pi\left(1 + \frac{1}{\frac{f_2}{f_1} - 1}\right)\right]$$

$$= \sin\left[2\pi + \frac{2\pi}{\left(\frac{f_2}{f_1} - 1\right)}\right] = \sin\left(\frac{2\pi}{\frac{f_2}{f_1} - 1}\right)$$

Therefore $\sin 2\pi f_1 t = \sin 2\pi f_2 t = \sin\left(\frac{2\pi}{\frac{f_2}{f_1} - 1}\right)$

The two frequencies would be phase coincident every $t = \left(\frac{1}{\frac{f_2}{f_1} - 1}\right)\frac{1}{f_1}$

$$= \left(\frac{1}{\frac{60.00}{59.94} - 1}\right)\left(\frac{1}{59.94}\right) \text{ sec}$$

$$= 16.67 \text{ seconds}$$

One solution to this problem would be to synchronize both color and monochrome cameras to the color vertical sync rate of 59.94 Hz. Thus color video would remain compatible with NTSC standards.

A more serious problem remains for color synchronization. There are two requirements for video synchronization:

(1) All cameras should sample video data in time-coincidence so that data reduction can be simplified.

(2) Time data should be available at each camera station so that it can be merged and recorded with video data.

Referring to Figures 3 and 4, recall that monochrome video cameras run at 60 fps. The timing unit provides 6 MHz, 2400 Hz, and 10 Hz signals which are used to produce 240 fps synchronized to a 10 Hz master reset. The 6 MHz is used to generate 1.26 MHz basic clock required by the camera sync generators. If the color cameras were to be synchronized in the same way, TABLE 1 shows what corresponding color video timing signals would be required. Present timing units do not provide the required color video timing signals

TABLE 1. COLOR VIDEO SYNCHRONIZATION REQUIREMENTS

| | Monochrome Video Timing Signals | Color Video Timing Signals |
|---|---|---|
| Timing Unit Signals | 6 MHz<br>2400 Hz<br>10 Hz | 3.579545 MHz<br>2397.6 Hz<br>9.99 Hz |
| Vertical Sync | 60 Hz | 59.94 Hz |
| Camera Sync Generator Clock | 1.26 MHz | 2.04545 MHz |

Suppose that only the camera sync generator clock is changed to 2.04545 MHz and all else remains the same. The 59.94 Hz vertical sync, produced by the generator would then drift in time with respect to the 10 Hz master reset signal of Figure 3. A disturbance would appear in the video image at a 10 Hz rate due to this drift.

The first synchronization requirement could still be met by broadcasting the first three signals shown in the second column of Table 1 to all camera stations. The second synchronization requirement could then be met by all stations sampling time data from presentl available units at multiples of 59.94 Hz up to a maximum of 239.76 Hz.

As a result of this analysis, conversations with a timing unit manufacturer revealed that the American Broadcasting Corporation (ABC) has standardized all color transmissions to 60 Hz vertical sync rates, and it is expected that the rest of the television broadcast industry will do the same. This means that manufacturers will make cameras compatible with this standard as well.

Meanwhile, present color cameras can be modified to work at 60 Hz vertical sync rates in anticipation of the industry standard. From this discussion it is evident that an IRIG video synchronization standard needs to be established to resolve the problem in a way that is acceptable to all interest parties.

## BINARY VIDEO INSERTER

Figure 8 shows the main functional blocks that make up the Binary Video Inserter (BVI). The Z8 microcomputer is used to read in time data from the timing unit at the beginning of every TV field, to read instrument encoder data from the DTF Z80 microcomputer, and to format and output the data to the timing and selection logic.

The data is formatted into a serial data stream of 1's and 0's, with the leading 23 bits as sync pattern. The on-board Z8 microcomputer makes it possible to change the format of the data, as data requirements change, by simply changing an EPROM.

### Timing and Insertion Circuits

This section is perhaps the most complex part of the BVI. A simplified block diagram is shown in Figure 9. The process begins by sampling the sync level (SL) and the blanking level (BL) at the beginning of every horizontal line of video. Signal $\overline{SBL}$ and $\overline{SSL}$ sample the blanking level and sync level, respectively. See Figure 10 to see how these two signals compare in time with the TV sync.

The summing amplifiers, following the sample-and-hold outputs, add multiples of the difference between BL and SL to the blanking level (SL-BL)X1 for a binary zero, and 5X(SL-BL) for a binary 1. The output video decoder selects one of the summing amplifier outputs depending on whether a "1" or a "0" data bit is at the output of the shift register during READ time. During the rest of horizontal-line-time, TV camera video is selected to be output.

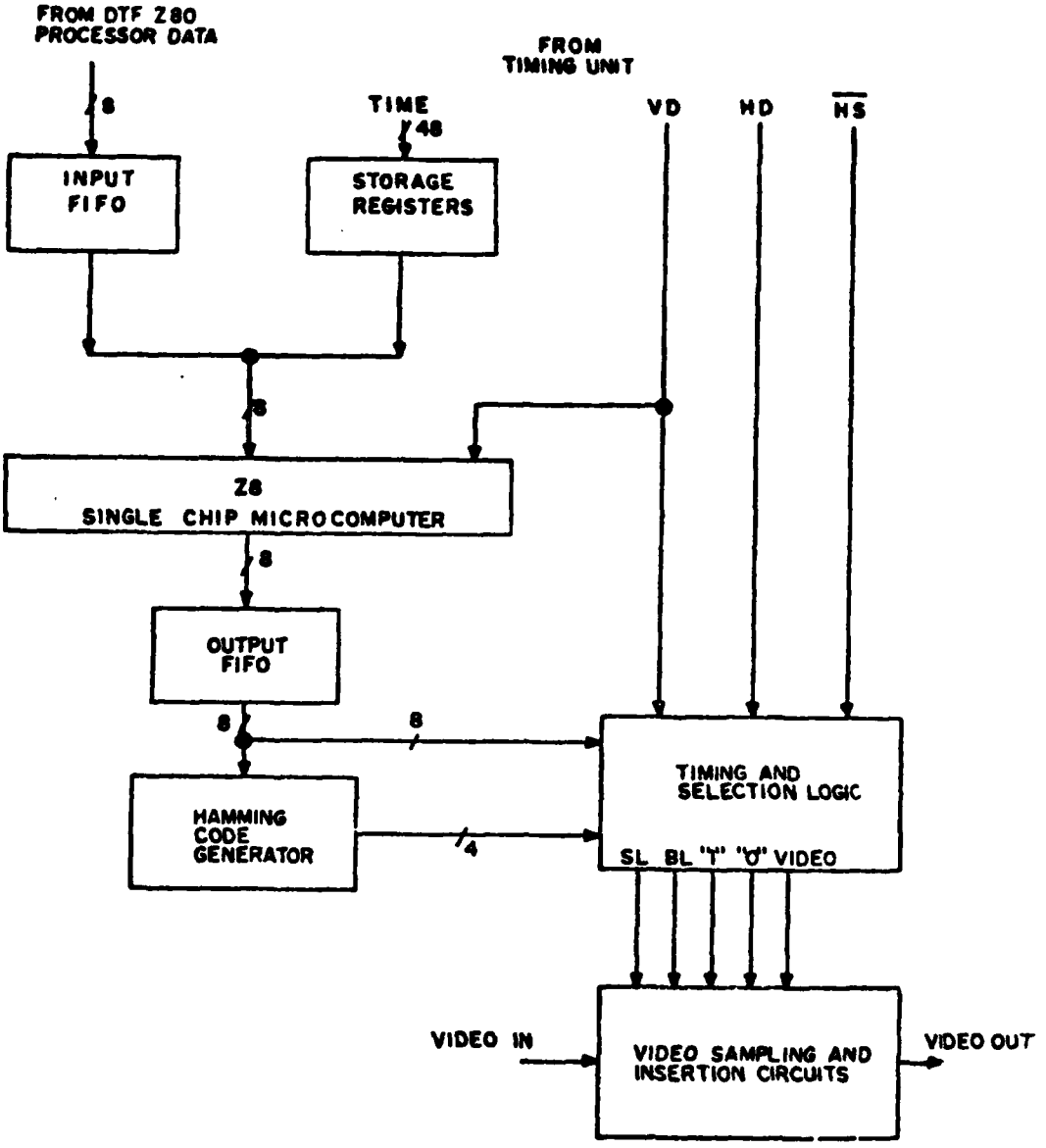



Figure 8. Binary video inserter block diagram.

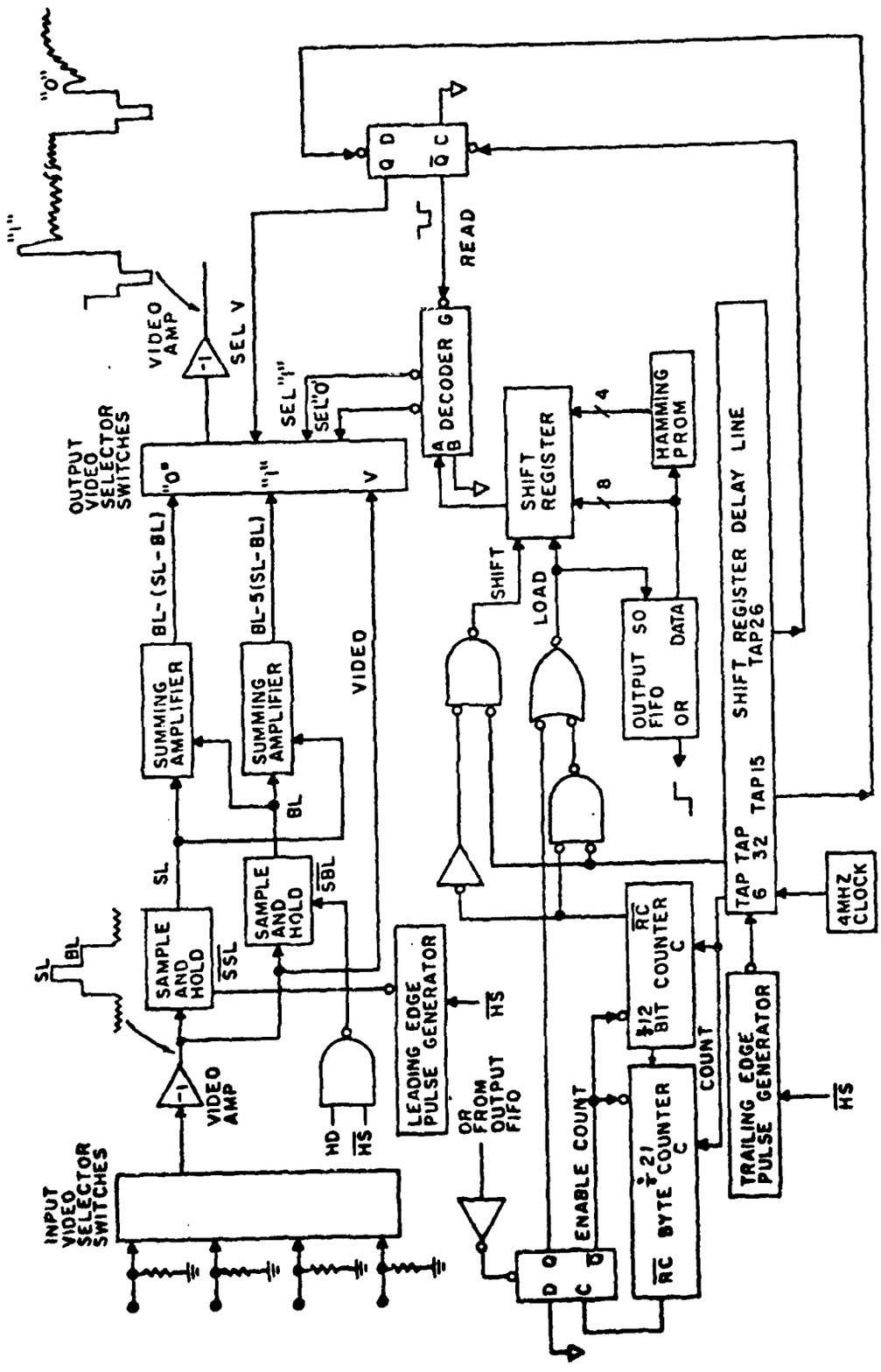



Figure 9. Video sampling, timing logic, and insertion circuits.

The lower half of Figure 9 contains the timing logic which automatically takes the data from the output first-in-first-out (FIFO) memory and loads it into the shift register. The leading edge of the vertical-drive (VD) signal latches time information from the timing unit and interrupts the Z8. The Z8 reads the contents of these latches, formats the data and outputs a block of data (containing the time) to the output FIFO. The output FIFO was empty before this block of data was entered. The first byte of data to reach the output side of the FIFO generates an output ready (OR) level, which presets the ENABLE COUNT flip-flop, causing the LOAD level to go high. This transition (of the load pulse) simultaneously traps the input data to the shift register and causes the output FIFO to begin the process of bringing out the next byte of data.

The ENABLE COUNT line also goes low, enabling the bit and byte counters to count. The first horizontal sync ($\overline{HS}$) to come along after VD goes away loads the shift register delay line with a pulse .75 microseconds wide. The delay line is tapped in four places to create the LOAD, COUNT, READ, and SHIFT pulses. The READ pulse is generated using TAP15 and TAP26, creating a pulse 11 clock (4 MHz) pulses wide. The READ pulse is 11 x .25 = 2.75 microseconds wide. The SHIFT pulse occurs after the READ pulse in order that the data at the shift register output does not change until after the data has been read and inserted into the video signal.

Taps 15 and 26 were selected for the READ pulse in order to position the binary data right on the trailing edge of the TV sync pulse. The sequence of events generated by the tapped delay line is: LOAD, COUNT, READ, SHIFT. The LOAD pulse is generated after every twelve READ, SHIFT pulses.

The SHIFT and LOAD pulses are both generated by TAP32 of the delay line. The BIT and BYTE counters are both down counters. When the BIT counter reaches count zero (meaning 12 lines of video have been counted) the BIT counter $\overline{RC}$ level goes low. This action prevents TAP32 from producing another SHIFT pulse and produces a LOAD pulse, instead. Thus, after every 12 shifts, the shift register gets loaded with new data. Since the BIT counter gets decremented before the READ pulse occurs, the first READ pulse after LOAD reads the data that was just loaded, and the process continues for the next twelve shifts.

After 21 words (12 bits long) have been counted by the BYTE COUNTER, the $\overline{RC}$ output from the BYTE COUNTER disables any further counting until the next video field begins, indicated by OR from the output FIFO. Thus, the timing logic always tries to write on 21 x 12 = 252 lines of video. If the FIFO contains less than 21 bytes, the logic will repeatedly write the last 12-bit word generated by the last byte of data in the OUTPUT FIFO until 21 bytes have been counted.

The first two 12-bit words written, following the VD signal, are used as a synchronization pattern. Actually, the first word is only 11 bits long, due to the BYTE COUNTER decrementing and the shift register shifting once during the VD interval. The second word and all following words are complete 12-bit words (see Figure 10).

## Z8 Programs

The on-board single-chip microcomputer basically services two interrupts. It gets interrupted 60 times per second by the VD signal from the TV camera sync generator. At this time the Z8 reads time data which has been latched with the leading edge of VD and reformats the time data into convenient eight-bit bytes for ease of processing by the data reduction computer.

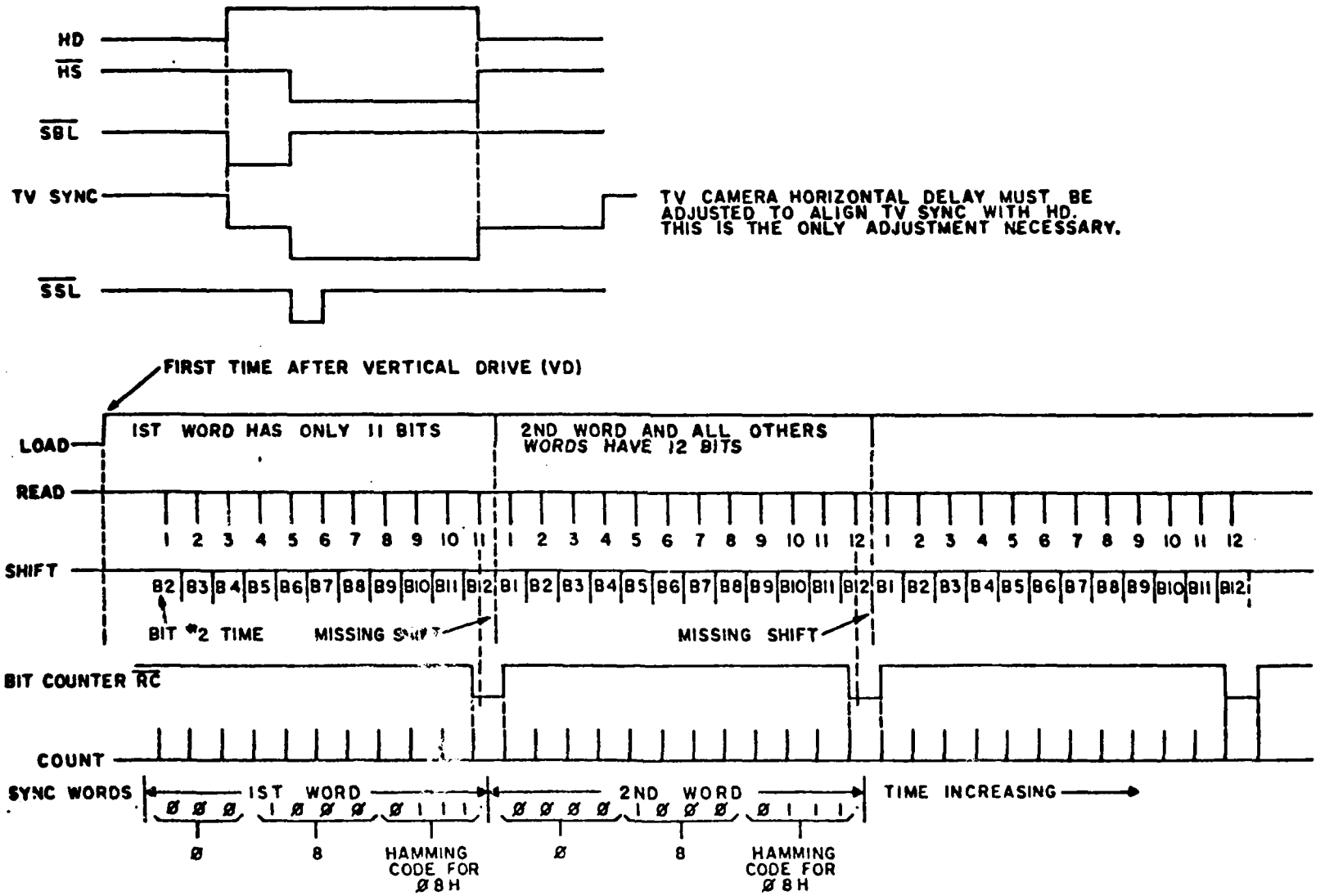



Figure 10. BVI timing generation.

The Z8 also gets interrupted 20 times a second by the DTF Z80 processor. At this time the Z8 reads the contents of the input FIFO and stores it in a common block of memory containing time data. The input FIFO contains instrument encoder data and any other status data that needs to be saved on video tape for data reduction purposes. See Figure 11 for a functional block diagram of the software.

## CONCLUSIONS

A prototype SBVI has been built and is presently being tested in the field. No error statistics are available yet.

There are, of course, other methods for inserting binary data into the video signal but none meet all of the needs identified in this report. There are promising developments in the commercial sector, however. The governments of England, France and Canada have each developed the Prestel, Antiope and Telidon systems, respectively, but there is no equivalent commercial standard in the United States. Each of these countries is trying to influence the United States to adopt its standard. In the meantime, AT&T has adopted a version of the Telidon standard. This may well become the defacto US Standard.

If the US adopts a standard, then low-cost LSI video processing circuits will become available to support it. For this reason, future SBVI units could be based on the US standard. The user would convert to the newer SBVI generation by simply pulling out the old board and inserting the new.

Datum, Inc., has developed a timing unit which incorporates digital data encoding into line 20 of the vertical blanking interval. Either 48 or 96 bits can be inserted on line 20 of each field; but it is not compatible with Teletext (Prestel, Antiope, Telidon). The performance of these units in terms of error recovery capability, immunity to time-base error, and immunity to burst noise errors is not known. The combination of a timing unit, together with digital data encoding and decoding built into the same package is an attractive combination, however.

WSMR data requirements are compatible with the method of data insertion presented in this report. WSMR development will, therefore, continue in its present direction.

Once present unknowns are resolved concerning error performance and video synchronization requirements, an IRIG video instrumentation standard will be needed to encourage production of low-cost commercial video instrumentation.

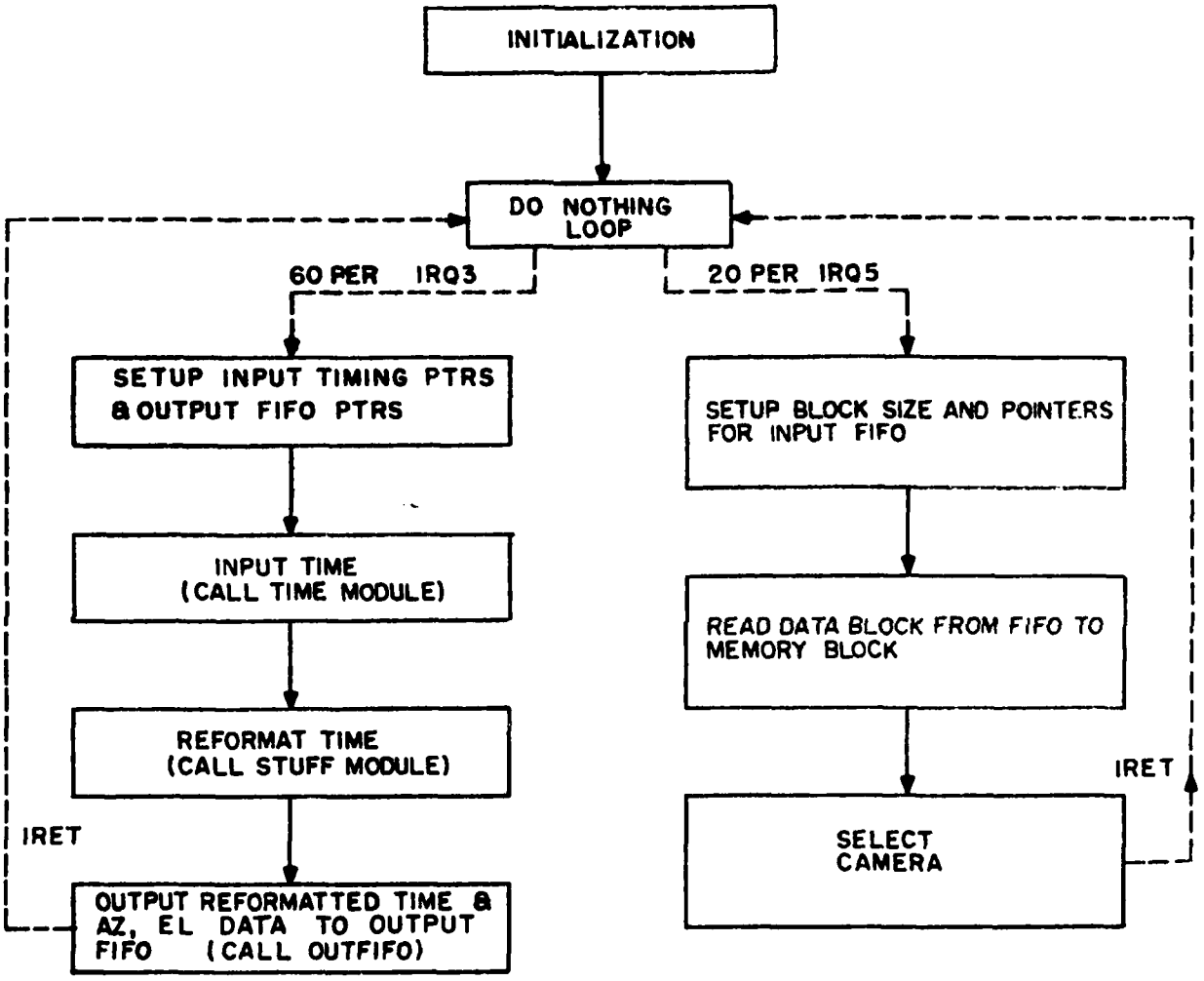



Figure 11. Z8 programs.

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